

Practitioner's Docket No. MIC-12693-1P

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of: Shekar Mallikarjunaswamy

Application No.: Filed Herewith                      Parent Appln. Group No.: 2818  
Filed: 09/19/2003                      Parent Appln. Examiner: Tu Tu V. Ho  
For: "THICK GATE OXIDE TRANSISTOR AND ELECTROSTATIC DISCHARGE PROTECTION  
UTILIZING THICK GATE OXIDE TRANSISTORS"

Mail Stop Patent Application  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Date: September 19, 2003

**INFORMATION DISCLOSURE STATEMENT**

**Identification of Prior Application in Which Listed Information Was Already Cited and for Which  
No Copies Are Submitted or Need Be Submitted**

This application relies, under 35 U.S.C. § 120, on the earlier filing date of prior application Serial No.:  
10/336,202, filed on 01/03/2003.

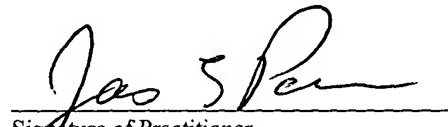
Copies of the documents listed on the accompanying Form PTO-1449 that are not enclosed were previously  
submitted in Application No. 10/336,202, from which this Application claims an earlier effective filing date.

Applicants respectfully request that the listed information be considered by the Examiner and be made of  
record in the above-identified application. If form PTO-1449 is enclosed, the Examiner is requested to initial and  
return it in accordance with MPEP § 609.

This statement is not intended to represent that a search has been made or that the information cited in the  
statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56.

Date: 19 Sep 03

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\_\_\_\_\_  
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James E. Parsons  
Bever, Hoffman & Harms, LLP

U.S. Department of Commerce, Patent and Trademark Office					Atty Docket No.		Application No.	
					MIC-12693-1P US		Filed Herewith	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT					Applicant(s)		Confirmation No.	
(Use several sheets if necessary)					Shekar Mallikarjunaswamy		Unknown	
					Filing Date		Group	
					Filed Herewith		Unknown	
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	4,109,274	8/22/1978	Belenkov et al.	357	38		
	AB	4,605,980	8/12/1986	Hartranft et al.	361	56		
	AC	4,745,450	5/17/1988	Hartranft et al.	357	23.13		
	AD	4,807,080	2/21/1989	Clark	361	56		
	AE	5,162,888	11/10/1992	Co et al.	257	108		
	AF	5,424,226	6/13/1995	Vo et al.	437	30		
	AG	5,504,444	4/2/1996	Neugebauer	327	108		
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	AJ	5,578,860	11/26/1996	Costa et al.	257	528		
	AK	5,602,404	2/11/1997	Chen et al.	257	112		
	AL	5,753,920	5/19/1998	Buehler et al.	250	370.06		
	AM	5,844,280	12/1/1998	Kim	257	355		
	AN	5,870,268	2/9/1999	Lin et al.	361	111		
	AO	6,064,249	5/16/2000	Duvvury et al.	327	314		
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL	WO 96/30936	3-Oct-1996	PCT				
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	AQ	Antinone, Robert J. et al., "Electrical Overstress Protection For Electronic Devices," Noyes Publications, pages 17-26.						
	AR	Pendharkar, Sameer et al., "SCR-LDMOS - A Novel LDMOS Device With ESD Robustness," 2000 IEEE, pages 341-344.						
		Wang, Albert Z.H. et al., "An On-Chip ESD Protection Circuit with Low Trigger Voltage in BiCMOS Technology," IEEE Journal of Solid-State Circuits, Vol. 36, No. 1, January 2001, pages 40-45.						
Examiner			Date Considered					
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.								

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U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
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	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
Foreign Patent Documents							
							Translation
		Document	Date	Country	Class	Subclass	Yes No
	AE						
	AM						
	AN						
	AO						
	AP						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
	AQ	Antinone, Robert J. et al., "Electrical Overstress Protection For Electronic Devices," Park Ridge, N.J., U.S.A.: Noyes Publications, 1986, pages 17-26.					
	AR	Iwamuro, N. et al., "Switching Loss Analysis Of Shorted Drain Non Punch-Through And Punch-Through Type IGBTs In Voltage Resonant Circuit," 3 <sup>rd</sup> International Symposium on Power Semiconductor Devices and ICS, ISPSD '91, April 22-24, 1991, pages 220-225.					
	AS	Simpson, M. R. et al., "Analysis Of The Lateral Insulated Gate Transistor," International Electron Devices meeting, Washington, D.C., December 1-4, 1985, pages 740-743.					
Examiner			Date Considered				
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							